REMARKS

The above amendments have been made to refer to the parent application and to make minor editorial changes so as to generally improve the form of the specification.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current Amendment. The attached page is captioned "**Version With Markings to Show Changes Made**".

Respectfully submitted,

Akihisa HONGO et al.

By _____

Nils E. Pedersen
Registration No. 33,145
Attorney for Applicants

NEP/krl
Washington, D.C. 20006-1021
Telephone (202) 721-8200
Facsimile (202) 721-8250
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In addition a copper pyrophosphate plating solution is also widely used because of its close adhesion due to high polarization and layered deposition property. However, copper pyrophosphate plating solution has poor leveling ability. Hence, when filling fine pits with copper in a plating process using copper pyrophosphate plating solution, the inlets to the fine pits become blocked first, thereby developing voids, as described above. Of course, it is also possible to use copper pyrophosphate plating solution as a first layer over a copper seed layer.

Disclosure of Invention

In view of the foregoing, it is an object of the present invention to provide a method and apparatus of plating a substrate capable of filling fine pits of channels and the like for fine wiring with copper, a copper alloy, or similar material having a low electrical resistance, such that the plating is uniform with no gaps and has a smooth surface.

These objects and others will be attained by a method for plating a substrate having a surface with fine pits formed therein, the method comprising/ performing a first plating process by immersing the substrate in a first plating solution having a composition superior in throwing power/ and performing a second plating process by immersing the substrate in a second plating solution having a composition superior in leveling ability.

With this method, a uniform initial plating layer without unplated areas on the side walls and bottom of the fine pits is

formed in the first plating process. A surface plating layer having a smooth surface and no void is formed on top of the initial plating layer in the second plating process.

According to another aspect of the present invention, the first plating solution is a high throwing power copper sulfate plating solution for printed circuit boards and the second plating solution is a copper sulfate solution. The high throwing power copper sulfate plating solution has a low concentration of copper sulfate, a high concentration of sulfuric acid, and is therefore superior in throwing power and coating uniformity. The copper sulfate plating solution has a high concentration of copper sulfate and a low concentration of sulfuric acid and is superior in leveling ability. As a result, plating metal is uniformly deposited on the surface of the semiconductor wafer, eliminating unplated areas formed on the side and bottom surfaces of the fine pits.

According to another aspect of the present invention, the high throwing power copper sulfate plating solution has a composition of 5-100 g/l of copper sulfate and 100-250 g/l of sulfuric acid, and the copper sulfate solution has a composition of 100-300 g/l of copper sulfate and 10-100 g/l of sulfuric acid.

According to another aspect of the present invention, a method for plating a substrate having a surface with fine pits formed therein and coated with a barrier layer, comprises performing a first plating process by immersing the substrate in a first plating solution having a composition superior in throwing power and in closely adhering to the barrier layer, and performing a second plating process by immersing the substrate

in a second plating solution having a composition superior in leveling ability.

With this method, a uniform initial plating layer without unplated areas on the side walls and bottom of the fine pits covered by the barrier layer is formed in the first plating process. A surface plating layer having a smooth surface and no void is formed on top of the initial plating layer in the second plating process.

According to another aspect of the present invention, the first plating solution is a copper pyrophosphate solution for printed circuit boards and the second plating solution is a copper sulfate solution. Due to the high polarization and the layered deposition property, the copper pyrophosphate sulfate solution forms a coating in close adherence with the barrier layer 5 formed of TiN or the like. The copper sulfate plating solution having a high concentration of copper sulfate and a low concentration of sulfuric acid is superior in leveling ability. Hence, this process forms a plating layer free of voids in the fine pits covered by the barrier layer, and the surface of the plating layer is smooth.

According to another aspect of the present invention, the copper sulfate solution has a composition of 100-300 g/l of copper sulfate and 10-100 g/l of sulfuric acid.

According to another aspect of the present invention, a substrate plating apparatus comprises a plating bath, first plating solution supplying means for supplying a first plating solution having a composition superior in throwing power to the plating bath, second plating solution supplying means for

supplying a second plating solution having a composition superior in leveling ability to the plating bath, and switching means for switching on and off the plating solutions supplied from the first and second plating solution supplying means.

With this construction, both the first and second plating processes can be performed in the same apparatus, since supply of plating solution is switched between processes, from the first plating solution superior in throwing power to the second plating solution superior in leveling.

According to another aspect of the present invention, the first plating solution has a composition with qualities superior for close adherence to a barrier layer formed on the surface of the substrate. With this construction, both the first and second plating processes can be performed in the same apparatus, since supply of plating solution is switched between processes, from the first plating solution superior in adherence to the barrier layer to the second plating solution superior in leveling.

Brief Description of Drawings

Figs. 1A-1C are cross-sectional diagrams showing the process for manufacturing a semiconductor element according to the substrate plating method of the present invention;

Fig. 2 is a flowchart showing the process of the plating method of the preferred embodiment;

Figs. 3A-3C are cross-sectional diagrams illustrating the process of Fig. 2;

Figs. 4A-4B are cross-sectional diagrams illustrating leveling ability;

Hence, when using a plating solution having superior leveling ability, film at the inlet to the fine pit 10 grows slow, as shown in Fig. 3B. This slow growth can prevent the generation of voids, thereby filling the fine pit 10 with a uniform layer of copper plating having no gaps. Moreover, it is possible to achieve a smooth surface on the plating.

Subsequently, the semiconductor wafer W is washed and dried to complete the plating process. This process achieves a plating layer 13 having a flat surface and free of voids. The fine pit 10 contains no unplated areas on its bottom or side walls.

Fig. 5 shows the construction of a plating apparatus suitable for the plating process described above.

The plating apparatus is provided with a plating bath 20, a first plating solution supplying section 22a ~~for~~ supplying a first plating solution 21 into the plating bath 20 and a second plating solution supplying section 22b ~~for~~ supplying a second plating solution 23 into the plating bath 20.

The first plating solution supplying section 22a includes a pump 24a for pumping first plating solution 21 into the plating bath 20, a shut-off valve 25a disposed upstream from the pump 24a, and a timer 26a ~~for~~ opening and closing the shut-off valve 25a.

Similarly, the second plating solution supplying section 22b includes a pump 24b for pumping second plating solution 23 into the plating bath 20, a shut-off valve 25b disposed upstream from the pump 24b, and a timer 26b ~~for~~ opening and closing the shut-off valve 25b.

In addition, a wash water supply tube 27 and a discharge

tube 28 are connected to the plating bath 20 for introducing wash water into the plating bath 20 and discharging wash water out of the plating bath 20, respectively. A pump 29 is connected to the tube 28.

As described above, a semiconductor wafer W, having undergone a preprocess, is inserted into the plating bath 20. Wash water is introduced into the plating bath 20 and the semiconductor wafer W is washed. Next, the shut-off valve 25a is opened according to the timer 26a. The first plating solution 21 is supplied into the plating bath 20, and the first plating process is performed. After a fixed time has elapsed, the shut-off valve 25a is closed. Wash water is again introduced into the plating bath 20 for washing the semiconductor wafer W. Subsequently, the shut-off valve 25b of the second plating solution supplying section 22b is opened according to timer 26b. The second plating solution 23 is supplied into the plating bath 20 and the second plating process is performed. Accordingly, it is possible to perform both the first and second plating processes consecutively using the same apparatus.

In the example described above, a timer is used for switching the supply of plating solution on and off. However, it is obvious that any means capable of performing this process can be used.

In the example described above, the same processing tank is used for performing the first plating process, the second plating process, and the washing processes. However, these processes can be performed using separate baths for each process. As shown in Fig. 9, for example, multiple baths can be provided,

Current density 2 A/dm^2

Plating time 2.5 min.

PH < 1

This process forms a plating layer 14 free of voids in the fine pit 10, as shown in Fig. 8A. No unplated areas are developed on the barrier layer 5 within the fine pit 10.

(First Comparison)

In a first comparison to the first embodiment, a semiconductor wafer W having undergone the same preprocess described above is plated using only the first plating solution. As shown in Fig. 8B, a void 30 is formed in the plating layer 14 within the fine pit 10.

(Second Comparison)

In a second comparison to the first embodiment, a semiconductor wafer W having undergone the same preprocess described above is plated using only the second plating solution. As shown in Fig. 8C, an unplated area 31 exists on the barrier layer 5 in a bottom corner of the fine pit 10.

In the first plating process of the present invention described above, a uniform initial plating layer without unplated areas on the side walls and bottom of the fine pit 10 is formed. In the second plating process of the present invention, a surface plating layer having a smooth surface and no void is formed on top of the initial plating layer. Accordingly, fine pits formed in the substrate, such as fine channels for wiring, can be filled with a copper, copper alloy, or other material having low electrical resistance without gaps in the metal plating and with an level surface.